

Warsaw University  
of Technology



Driver module for quantum computer  
experiments - Kasli

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Thesis supervisor:

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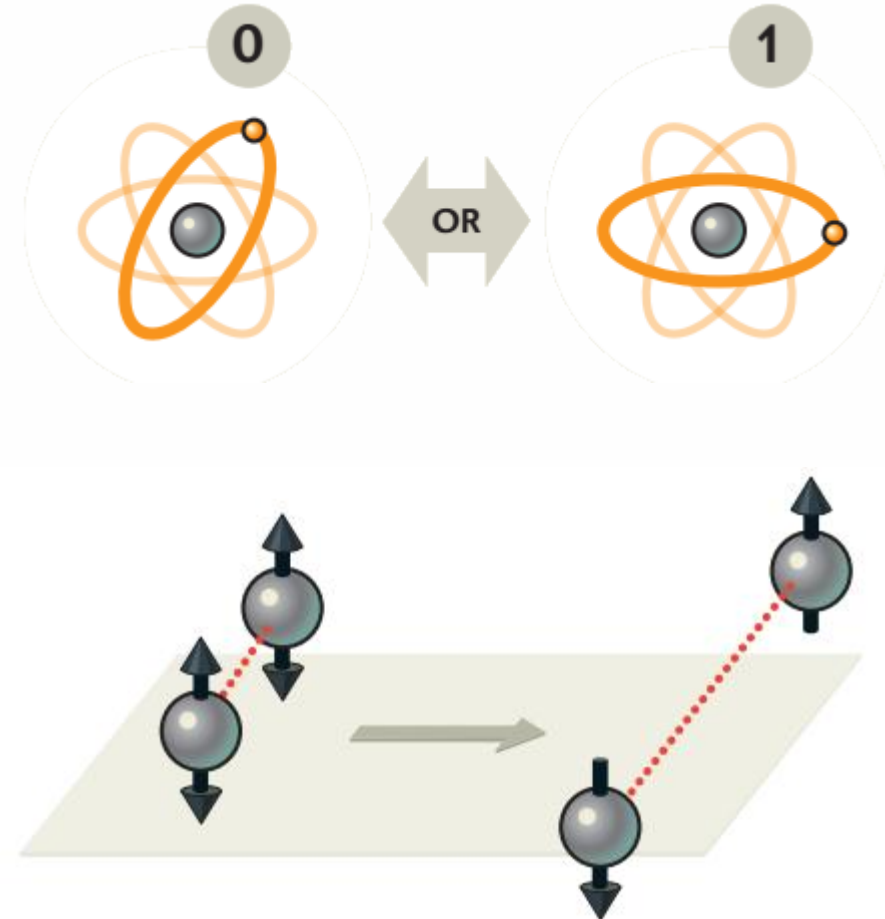


# Quantum computer research

- Why does it matter
  - Finding new prime numbers
  - Breaking current encryption (factorization)
  - Quantum versions of classical algorithms

# Quantum computer research

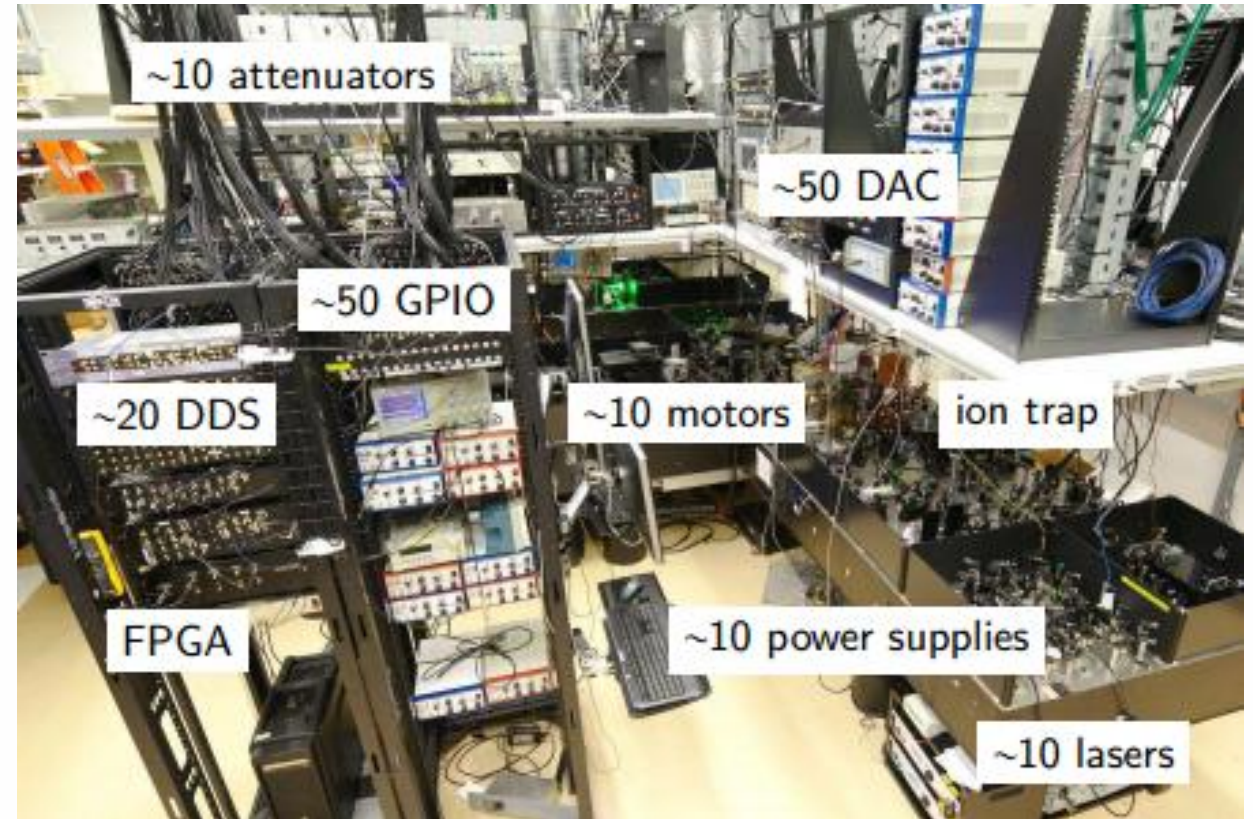
- Why does it matter
- Qubits
  - Superposition
  - Entanglement
  - Difficulties in maintaining superposition



Source: Scientific American, May 2016

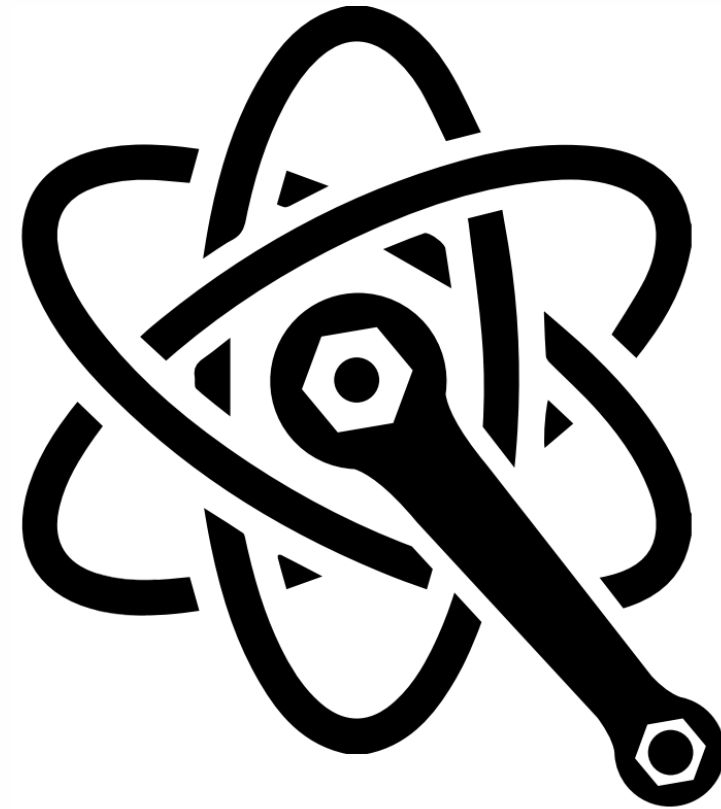
# Quantum computer research

- Why does it matter
- Qubits
  - Superposition
  - Entanglement
  - Difficulties in maintaining superposition
- Electronics involved in research



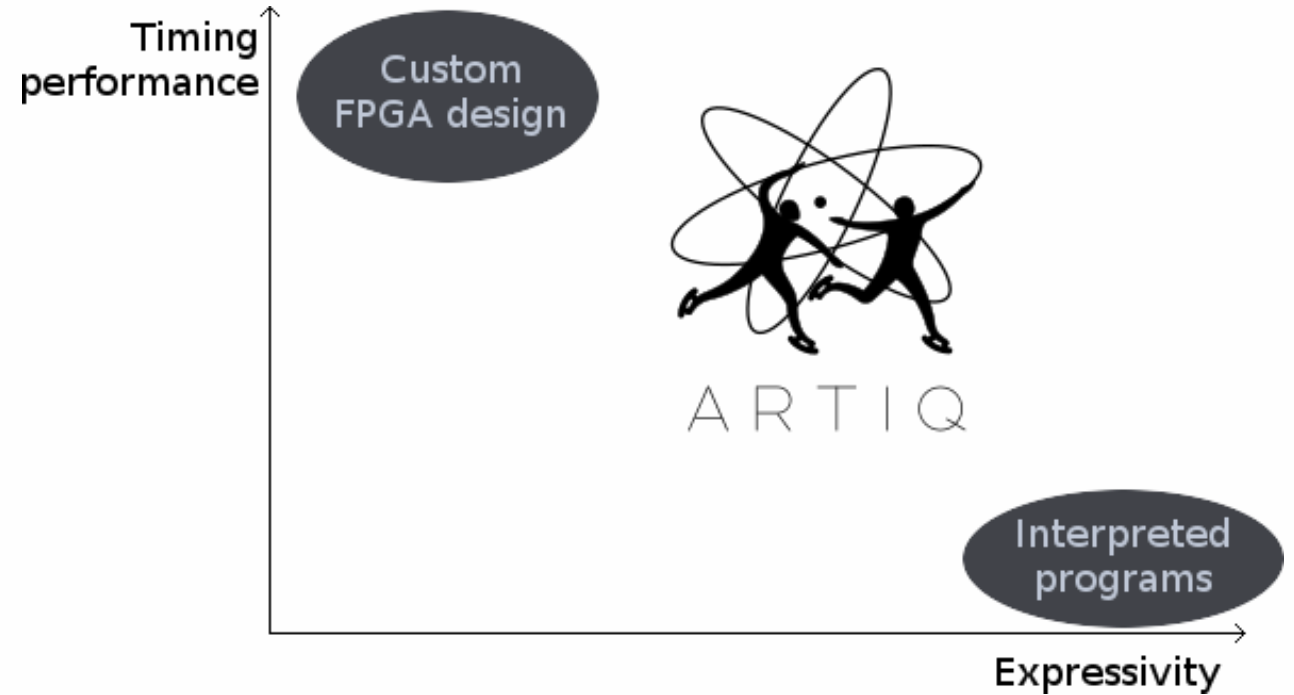
Source: m-labs.hk

- Advanced Real-Time Infrastructure for Quantum physics
- High-level programming language for describing complex experiments



# ARTIQ

- Advanced Real-Time Infrastructure for Quantum physics
- High-level programming language for describing complex experiments
- Time-critical code running on FPGA



Source: m-labs.hk

- Advanced Real-Time Infrastructure for Quantum physics
- High-level programming language for describing complex experiments
- Time-critical code running on FPGA
- Other code running on PC controlling the experiment

The screenshot displays the ARTIQ control interface with several key components:

- Top Left:** A plot titled 'Applet: flopping' showing a signal with a sharp dip around 1500. Below it, a digital display shows '1500.00469'.
- Top Middle:** A control panel for 'repo:ArgumentsDemo' with fields for 'Integer' (42) and 'string' ('Hello World'). It includes scan mode options (No scan, Linear, Random, Explicit) and a 'Flux capacitor' section with a frequency slider set to 95.8 kHz.
- Top Right:** A TTL status table with columns for various TTL signals (ttl0 to tt1) and their current states (OUT, IN).
- Bottom Left:** A log window showing system messages and error/warning logs from 'worker(2171.arguments\_demo.py)'. One error message is highlighted in red: 'root:logging test: error'.
- Bottom Right:** Two histograms: one showing a distribution of data points (marked with 'x') and another showing a frequency distribution.

Source: m-labs.hk

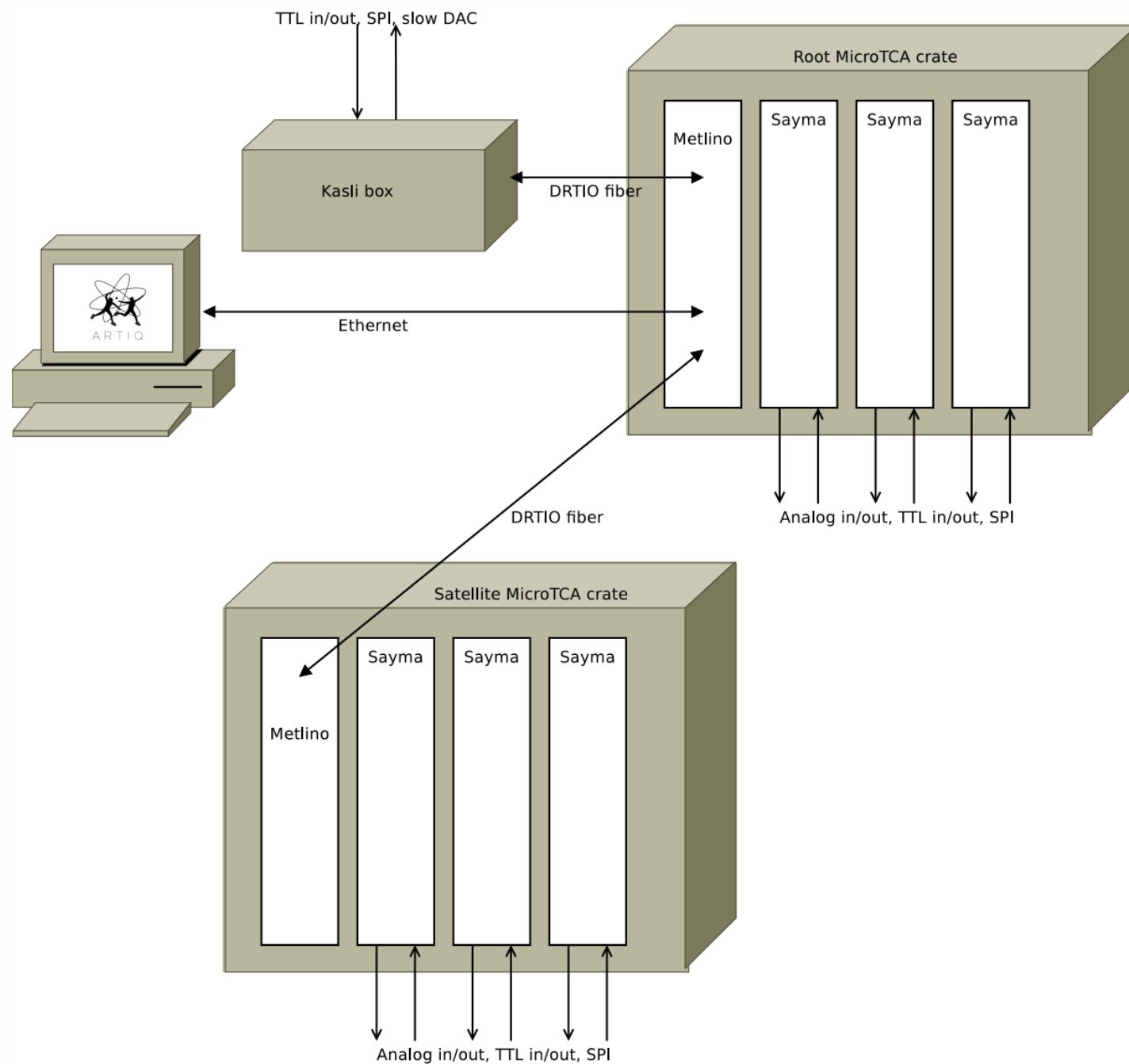
- High quality hardware for ARTIQ
  - Modular
  - Flexible
  - Well tested
  - Open source



- High quality hardware for ARTIQ
- International cooperation
  - M-Labs (Hongkong)
  - University of Oxford
  - Warsaw University of Technology
  - University of Maryland
  - NIST Boulder (USA)

# Sinara

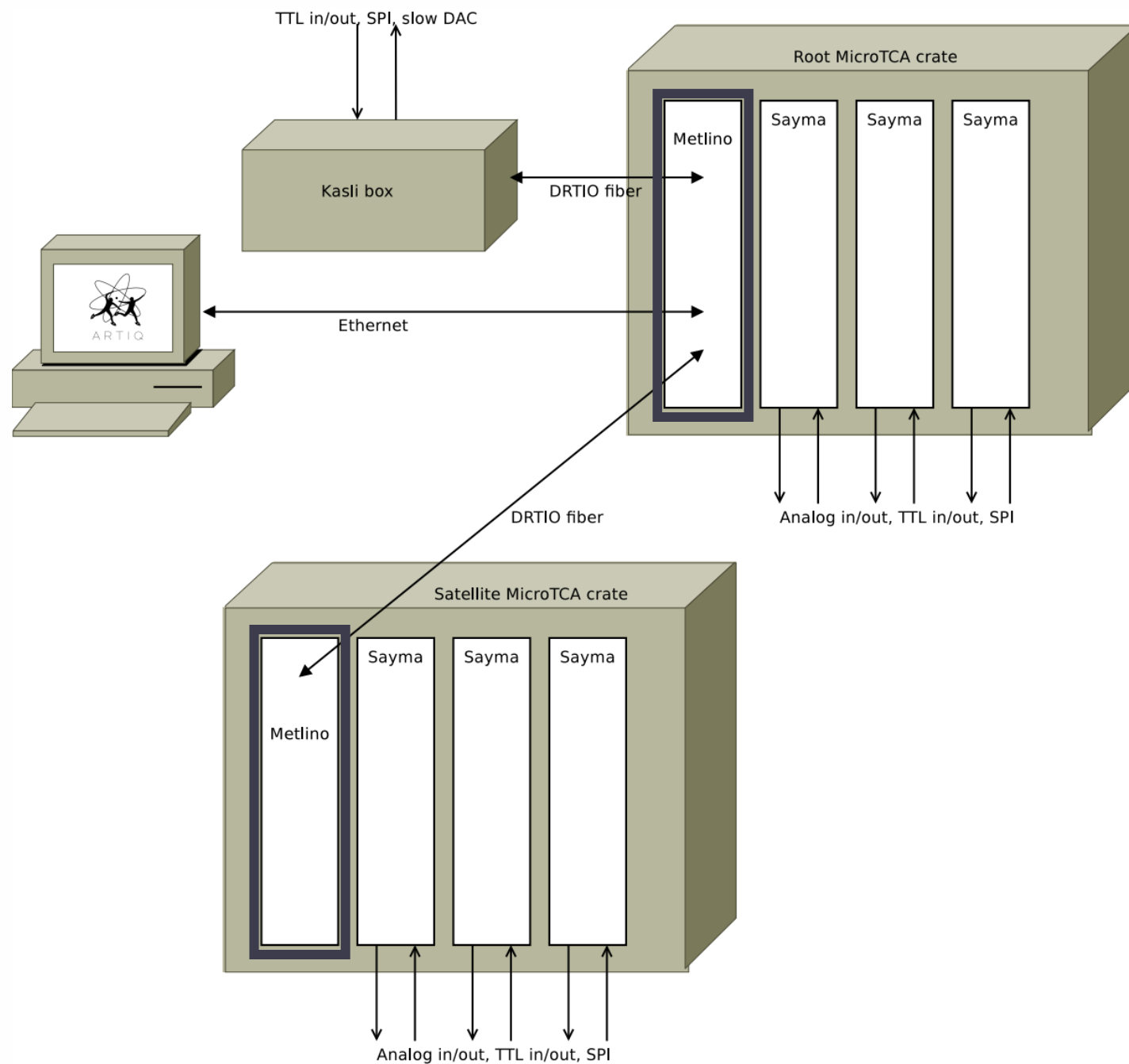
- High quality hardware for ARTIQ
- International cooperation
- System architecture



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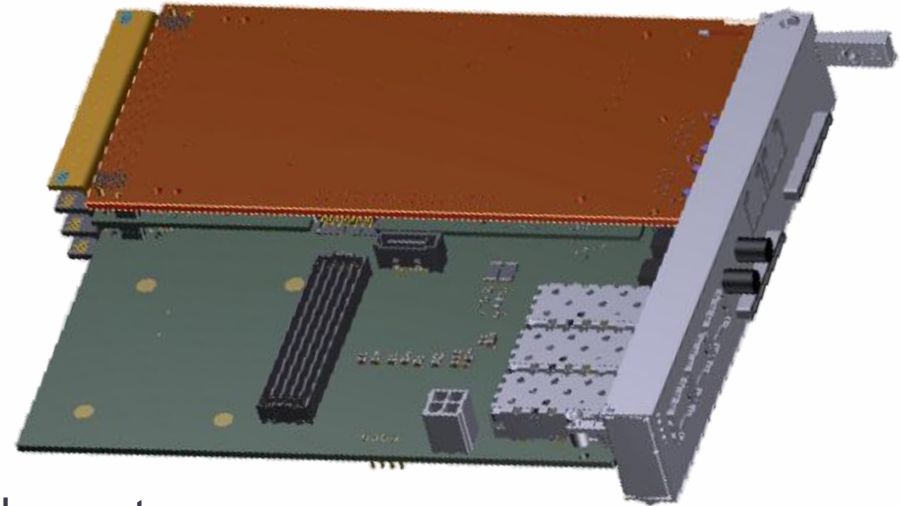
# Sinara

- High quality hardware for ARTIQ
- International cooperation
- System architecture
  - Metlino



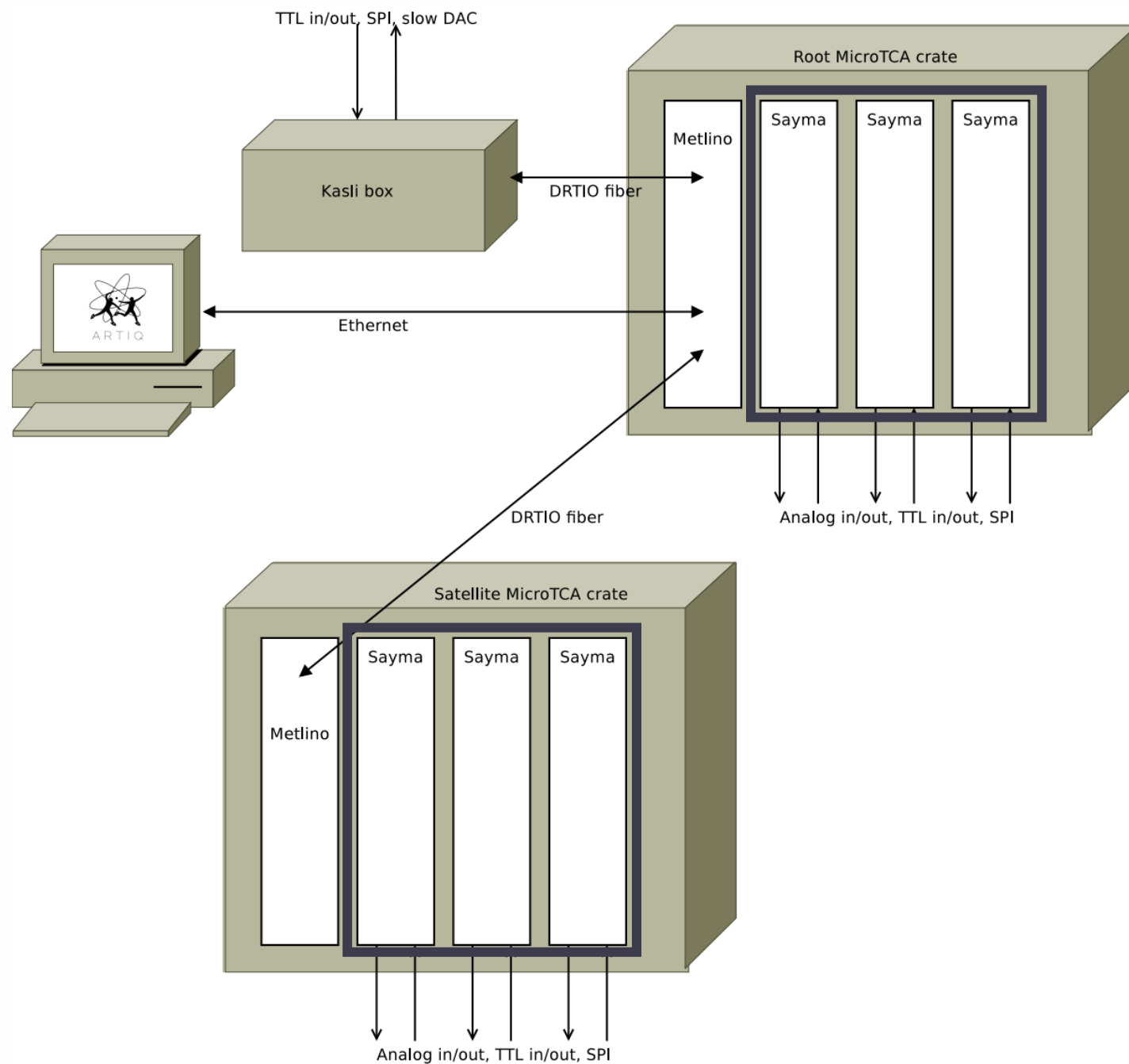
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- High quality hardware for ARTIQ
- International cooperation
- System architecture
  - Metlino
    - distributes DRTIO commands to the other cards in the crate over the MicroTCA backplane (star topology)
    - distributes DRTIO commands to other crates
    - receives commands from another Metlino board or control PC

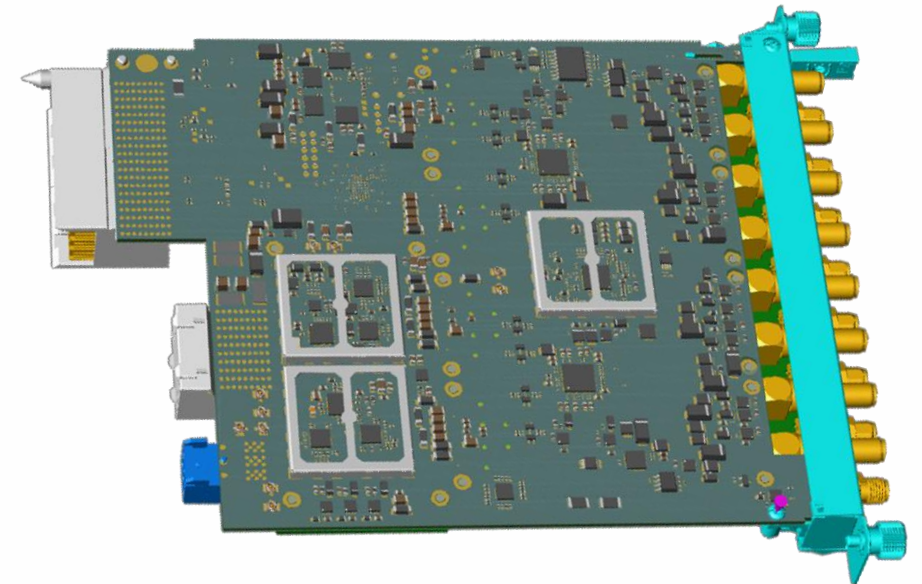
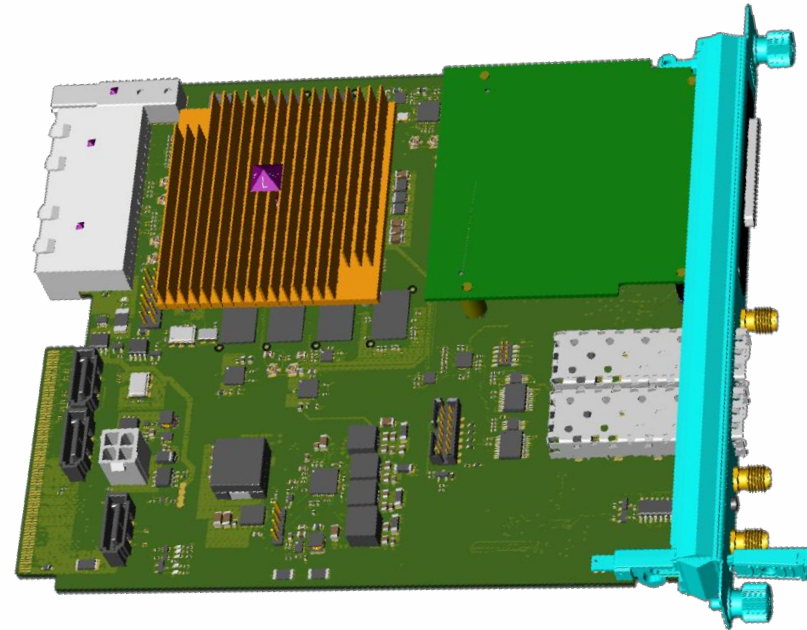


# Sinara

- High quality hardware for ARTIQ
- International cooperation
- System architecture
  - Metlino
  - Sayma

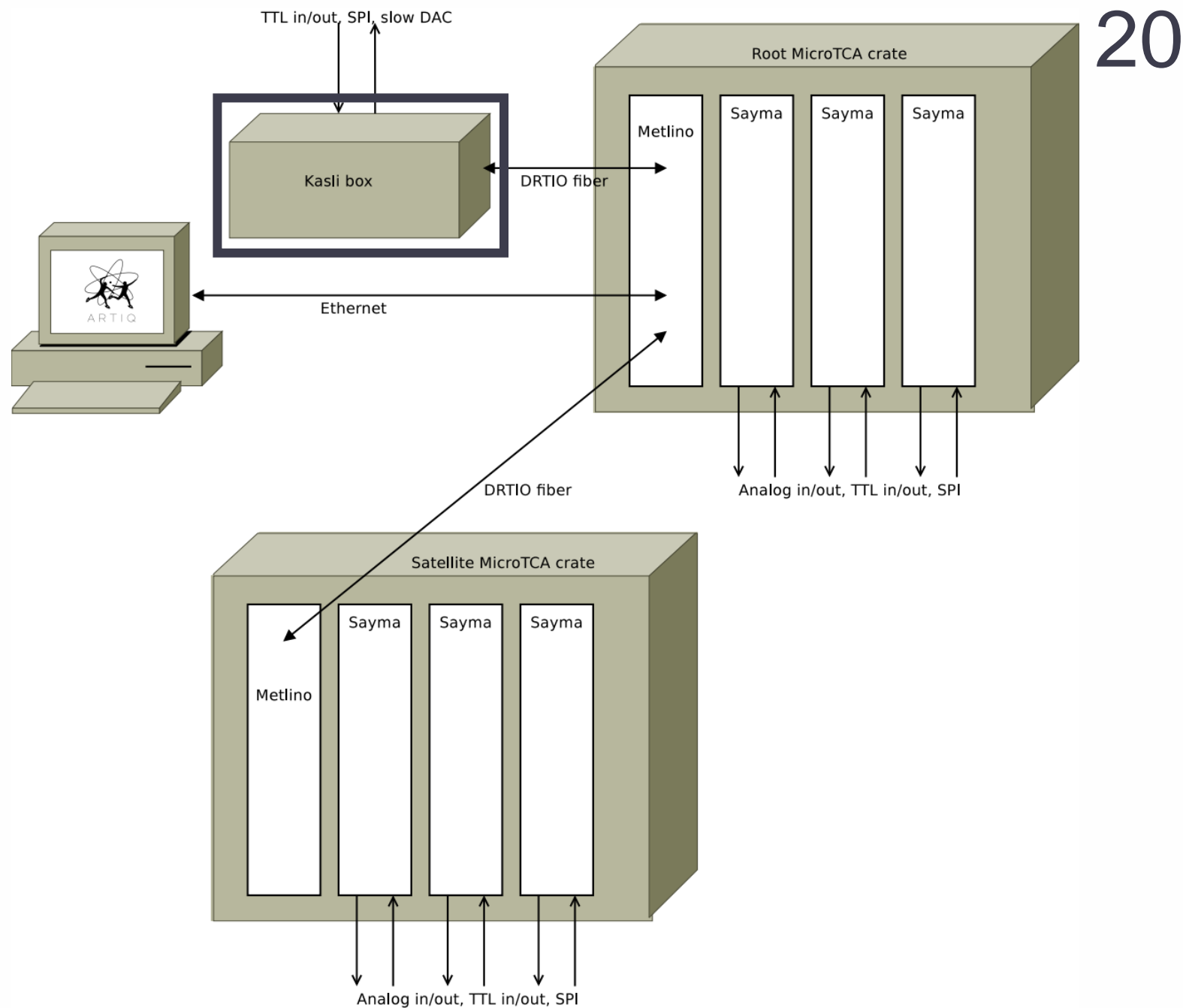


- High quality hardware for ARTIQ
- International cooperation
- System architecture
  - Metlino
  - Sayma
    - Extension cards that contain a FPGA
    - Typically used to generate and process RF signals
    - ADCs and DACs are on uRTM extension
    - Optional FMC extension

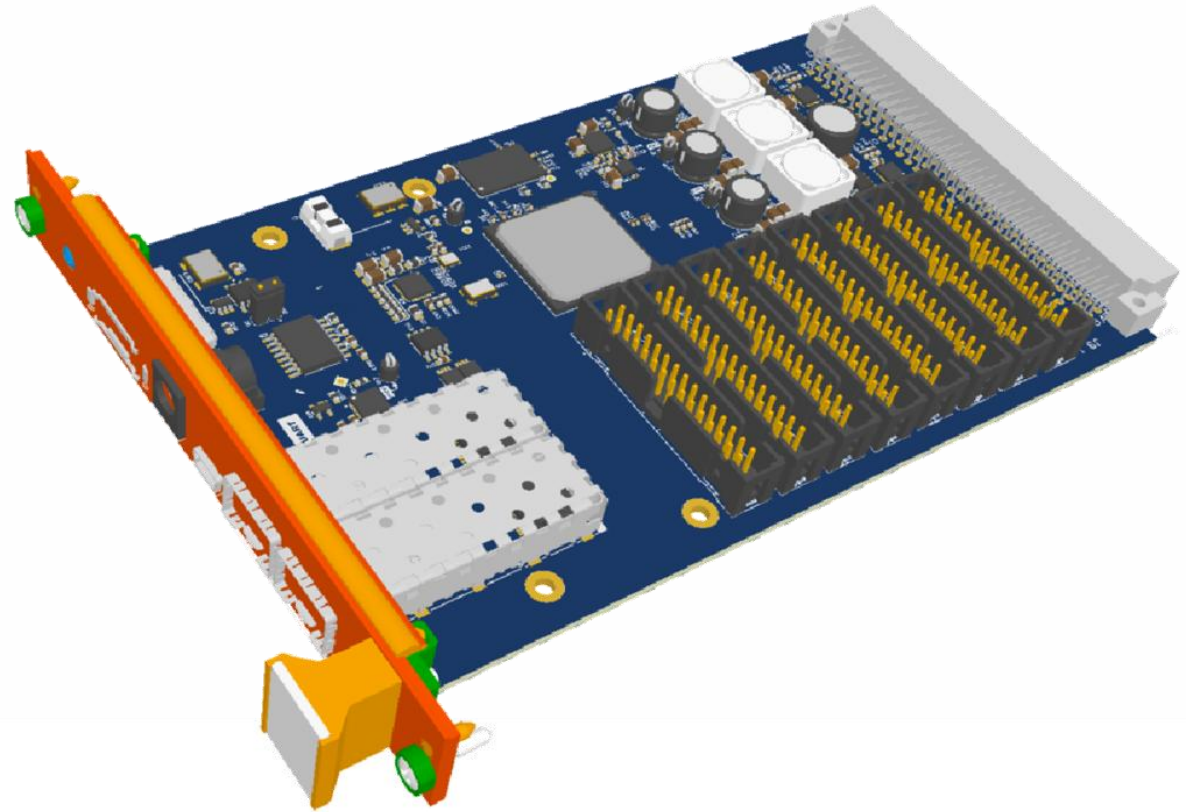


# Sinara

- High quality hardware for ARTIQ
- International cooperation
- System architecture
  - Metlino
  - Sayma
  - Kasli

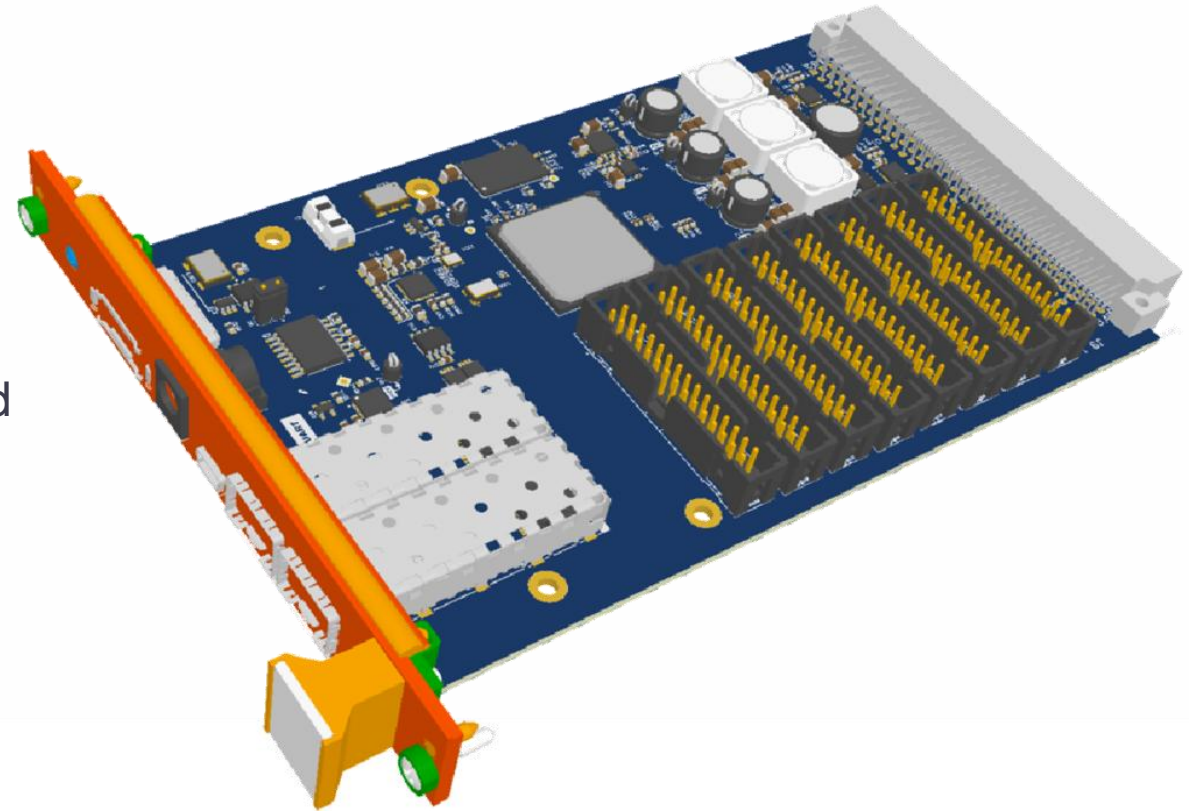


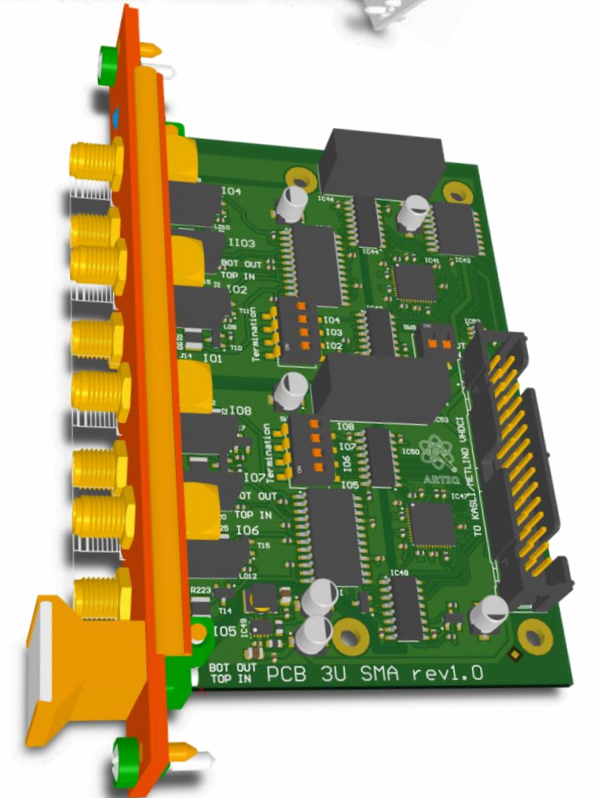
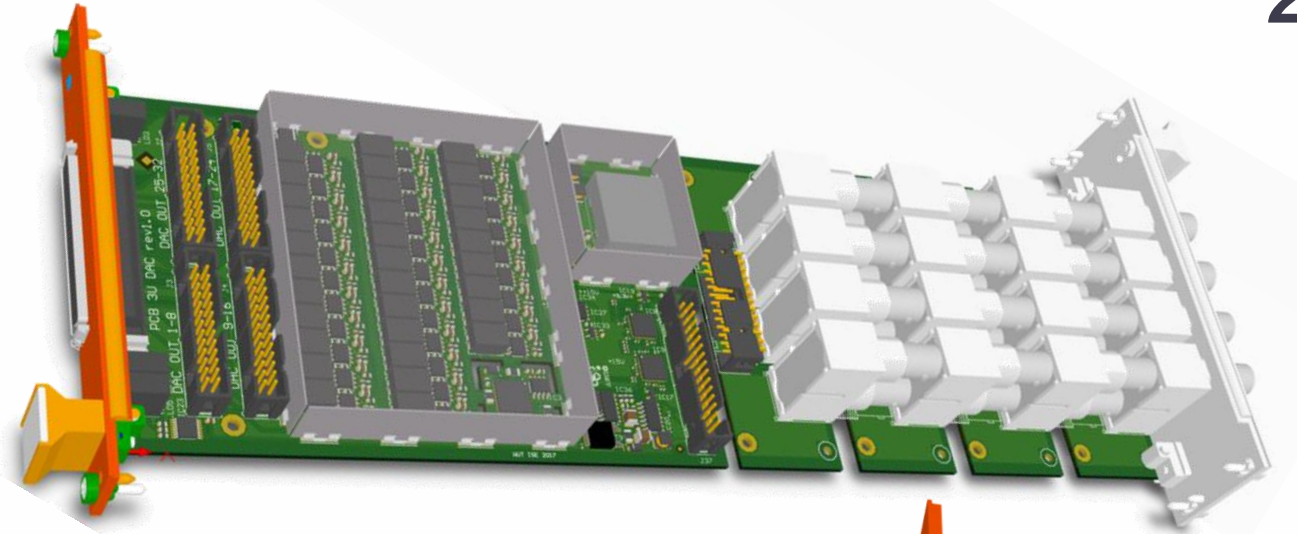
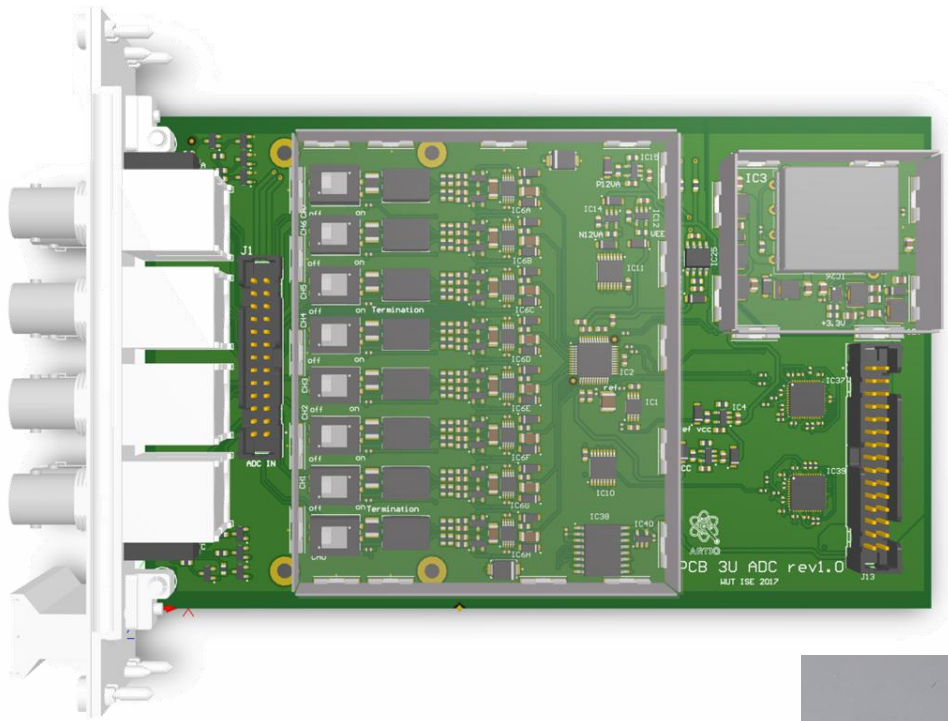
- My area of work
- Controls external equipment, that doesn't require precision provided by Sayma



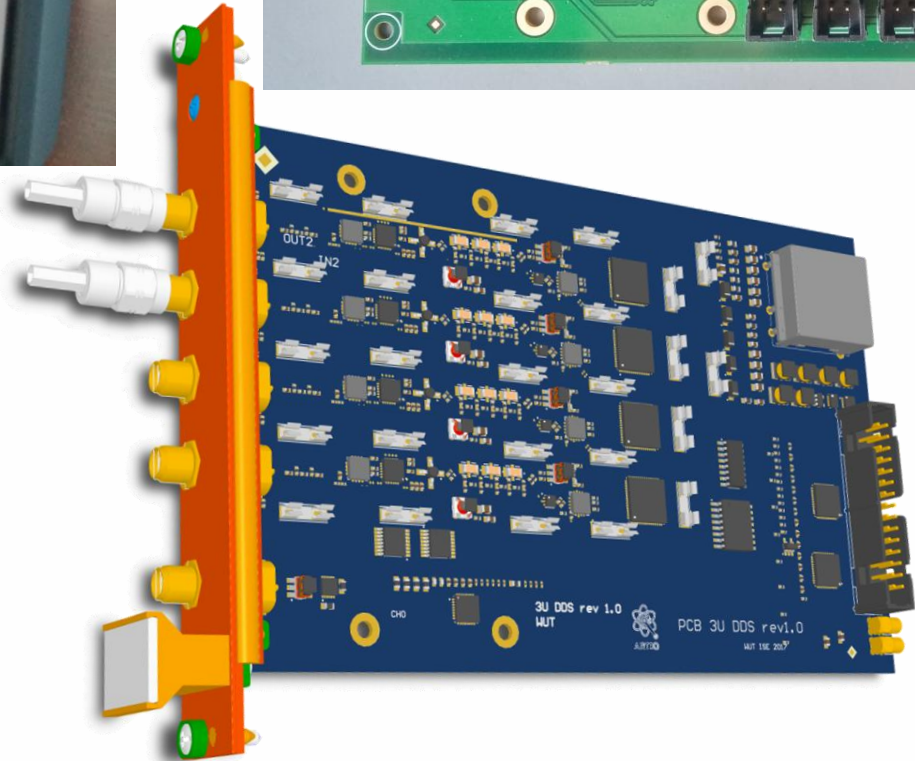
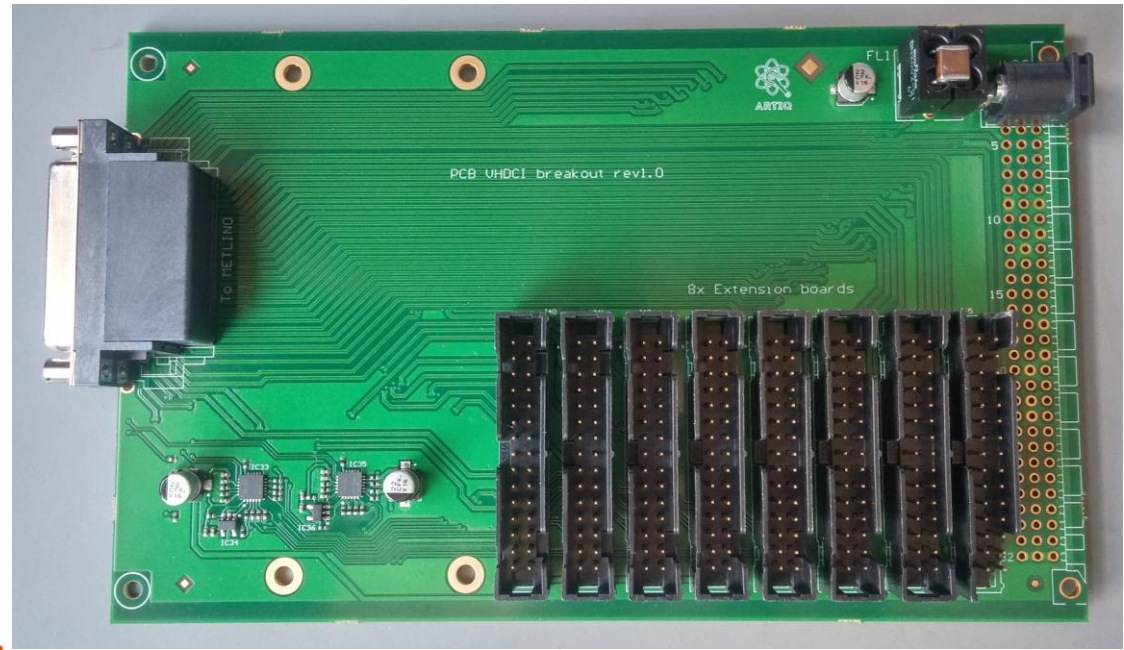


- My area of work
- Controls external equipment, that doesn't require precision provided by Sayma
- Receives DRTIO commands from master (Metlino) card
- Up to 12 extensions
- Extensions may be connected by ribbon cables (backplane is scrapped ... for now)



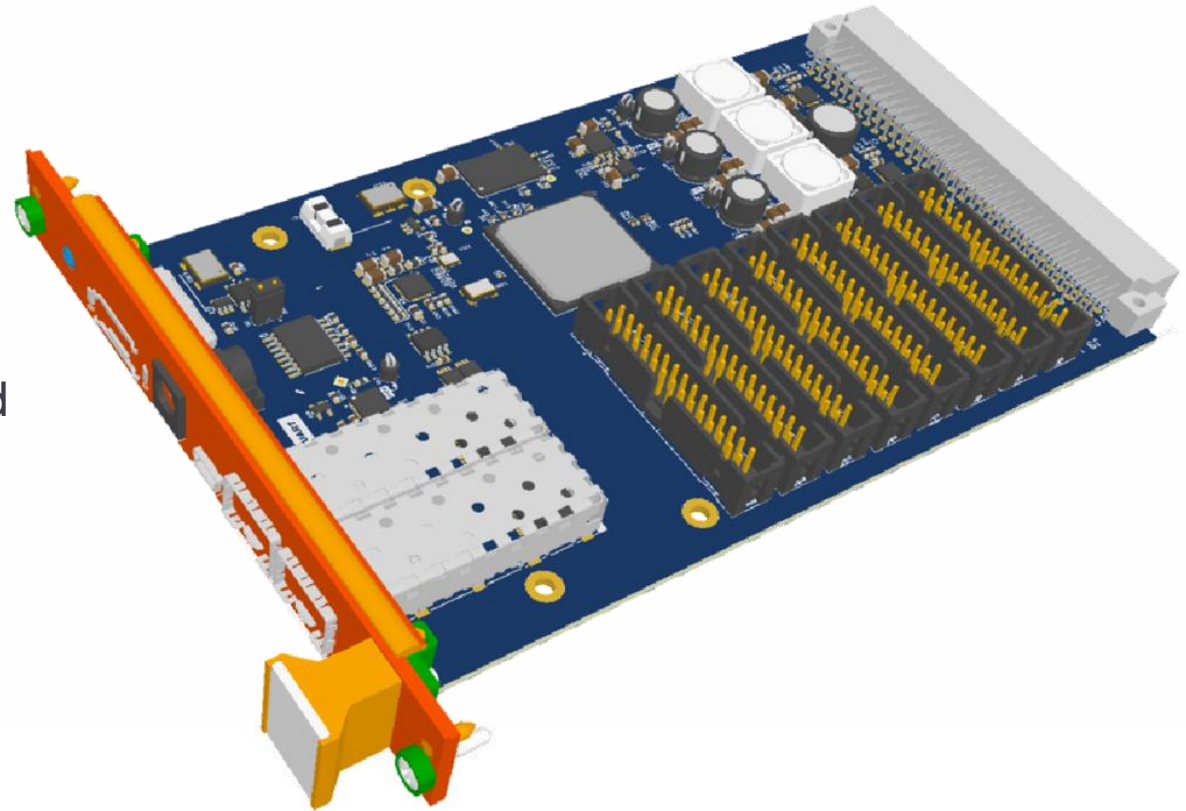


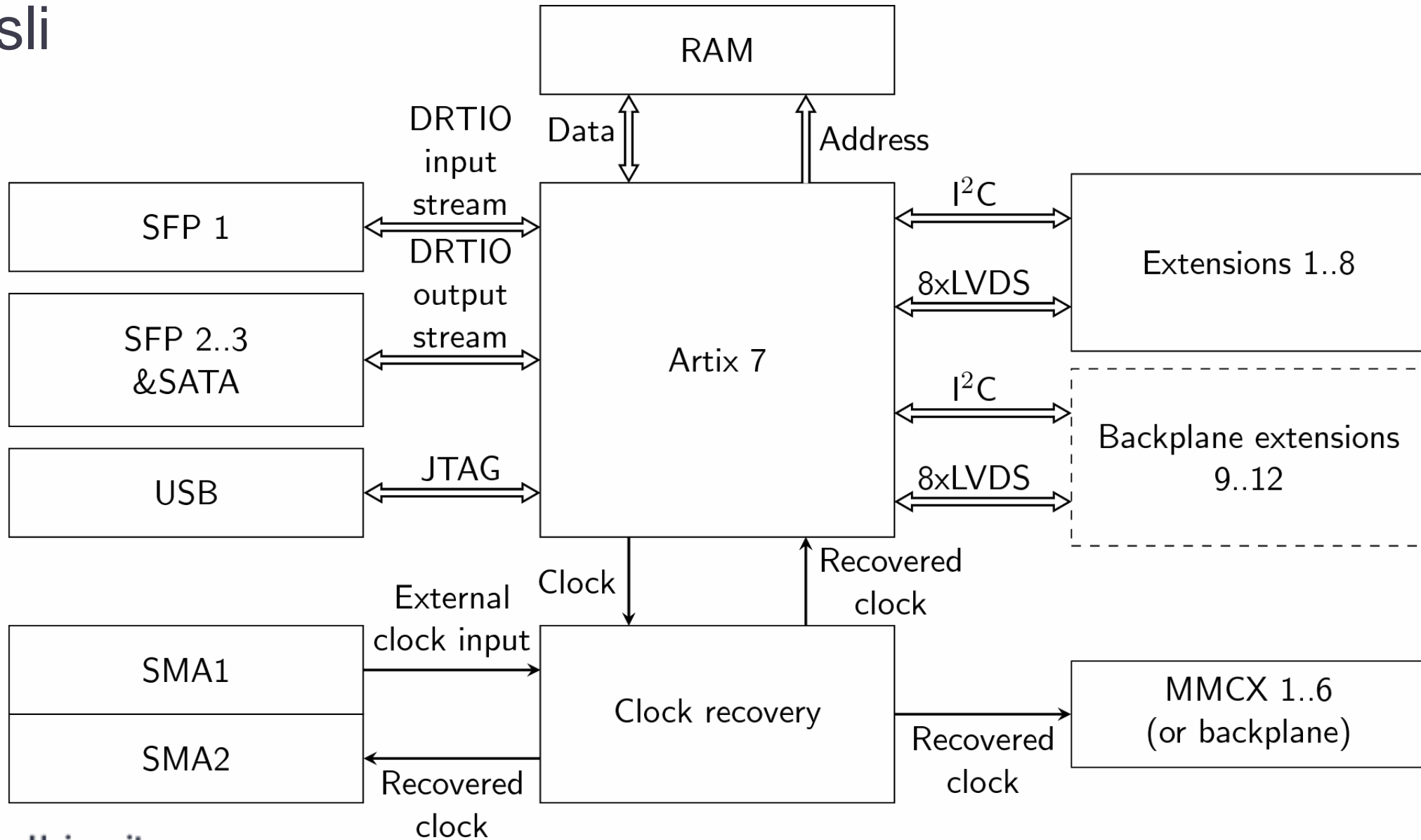
Examples of extensions



Examples of extensions

- My area of work
- Controls external equipment, that doesn't require precision provided by Sayma
- Receives DRTIO commands from master (Metlino) card
- Up to 12 extensions
- Extensions may be connected by ribbon cables
- Rough specification and use cases are agreed upon





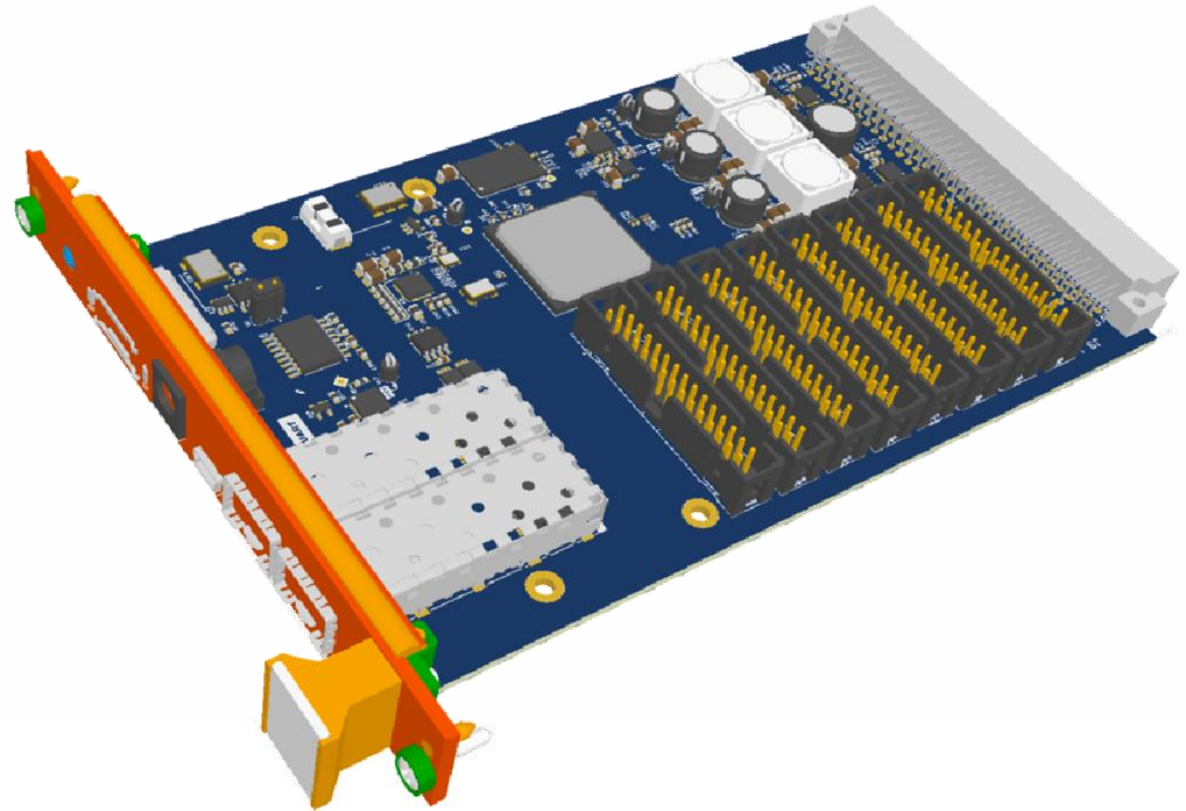
Progress:

- Rough specification
- Electrical schematics

What remains to be done:

- PCB project
- Simulations
- Physical tests

Whole project is on GitHub: [github.com/m-labs/sinara](https://github.com/m-labs/sinara)



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